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THE INTEGRATION OF NOC ARCHITECTURE WITH CLASSICAL BUS-BASED SYSTEMS

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ABSTRACT

The increasing complexity of modern digital devices demands for ever increasing communication requirements, and for an ever increasing heterogeneity of the target applications. Specifically, different communication domains may be implemented using the same chip area, for instance to allow multiple parallel applications to be loaded onto the device. Network-on-Chip (NoC) architectures represent a promising design paradigm to cope with increasing communication requirements in heterogeneous digital systems. Classical design approaches, such as bus-based systems or point-to-point connections, are no longer suitable for highly integrated systems since they lack of flexibility and scalability with the increasing number of modules attached to the system. Nevertheless, NoC-based interconnects require additional design efforts and, in general, major resource requirements as compared to classical bus-based systems. Such an issue can be solved by directly optimizing over the different design factors. What should be achieved is low-resource usage communication architecture, meanwhile maintaining the desired performances. In the proposed methodology Integration of NoC (Network on Chip) architecture with Classical Bus based systems to overcome the disadvantages of both Classical and Network based methodologies. The efficiency of the proposed methodology is shown by comparing with existing methodology, taking directly into consideration the resource requirements of the target FPGA device.

KEY WORDS: System on chip, Network-on-chip, Communication requirements, Point to point connection, Bus based systems.